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EXAMINER	
SUGENT, JAMES F	

ART UNIT	PAPER NUMBER
2116	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/764,406	NEWMAN, PAUL F.	
	Examiner	Art Unit	
	James Sugent	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1 and 23-24 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Ovens et al. (U.S. Patent No. 6,351,173 B1) (hereinafter referred to as Ovens).

As to claim 1, Ovens discloses an apparatus, comprising: a clock source (clock tree synthesis circuit, not shown in Ovens, and hereinafter referred to as CTS) to generate a clock signal (clock signal 108 in core 104); a first circuit (core 104), coupled to a first supply voltage source (V_{DD}), to generate a first data signal (output Q 122) and a second circuit (I/O 102) coupled to a second supply voltage source (V_{DDS}) (column 3, lines 43-61); a first level shifter (206 in I/O 202), coupled to the first circuit (from output Q 122 of core 104 or output from core 200 as signal A 204; column 4, lines 35-43), to generate a level shifted data signal (shifting from voltage level V_{DD} to voltage level V_{DDS}) in response to the first data signal (Ovens discloses the input signal from the core 200 being level shifted by level shifter 206; column 4, lines 35-43 and column 4, lines 50-59); and a downstream latch (master latch in Box B of figure 2), having a pair of inputs (clock signals CLKT or CLKF and data signal Y 222 received from the output of Box A in figure 2) coupled to the first level shifter (206 in Box A) and the clock source (signals generated from the CTS from signal 208 to signals CLKT and CLKF) and an output coupled to

the second circuit, to generate an output data signal (output signal Q in figure 2) in response to the level shifted data signal (from level shifter 206) and the clock signal (CLKT or CLKF) (Ovens discloses the data signal entering the I/O 202 is level shifted by level shifter 206 and latched by master and slave latches [Box B and transistors M11-M14 in figure 2] to output Q as is also depicted in figures 4a-c; column 5, lines 11-33 and column 5, line 66 thru column 6, line 14).

As to claim 23, Ovens discloses a method, comprising: supplying a first supply voltage (V_{DD}), a second supply voltage (V_{DDS}), and a clock signal having a rising clock edge and a falling clock edge (CLK 108); shifting (via level shifter 206 in I/O 202) a first data signal (from output Q 122 of core 104 or output from core 200 as signal A 204; column 4, lines 35-43) from the first supply voltage to the second supply voltage by way of a first level shifter (Ovens discloses a level shifter 206 shifting the signal from the voltage level of the core 200 of 1.8 volts [VDD] to the voltage level within the I/O 202 of 3.3 volts [V_{DDS}] with output of signal Y 222 as shown in figure 2; column 4, lines 35-43); generating a level shifted data signal from the first level shifter with the level shifted data signal having a plurality of rising and falling data edges that are mismatched (Ovens discloses the level shifting circuit and clock signals within the I/O section comprising mismatched signals due to the delays between the level shifting and clock signals [clock-to-Q]; column 4, lines 20-28); and latching (in master latch in Box B of figure 2) the level shifted signal (signal Y 222) in response to one of the rising and falling clock edges (CLKT or CLKF) after the rising and falling data edges have occurred (column 5, lines 11-33).

As to claim 24, Ovens discloses the method wherein latching (done by master and slave latches, as discussed hereinabove) the level shifted data signal includes using a downstream latch

to latch the level shifted data signal after the rising and falling data edges have reached the latch (column 5, lines 34-45 and column 5, line 66 thru column 6, line 14).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 10-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ovens et al. (U.S. Patent No. 6,351,173 B1) (hereinafter referred to as Ovens) in view of Cairns et al. (U.S. Patent No. 6,806,734 B2) (hereinafter referred to as Cairns).

As to claim 10, Ovens discloses an apparatus, comprising: a microprocessor including a central processing unit (CPU) section having a first supply voltage source (V_{DD}) (see figures 1 and 2); an input-output (I/O) section having a second supply voltage source (V_{DDS}) (see figures 1 and 2); a clock source to generate a clock signal (108 of figure 1 or 208 of figure 2; column 3, lines 43-50); and a selected section of the CPU section (core 104 or 200; see figures 1 and 2) and the I/O sections (I/O 102 or 202; see figures 1 and 2) being operable to generate a first data signal (Ovens discloses the core 104 providing an input data signal A 204 before processing onto I/O section for outputting; column 4, lines 35-43); a converter circuit including a first level shifter (206), coupled to the selected section (coupled to both the core and the I/O sections), to generate a level shifted data signal in response to the first data signal (column 4, lines 35-43);

and a downstream latch (Box B of figure 2 within the I/O section), having a pair of inputs (clock signals CLKT or CLKF and data signal Y 222 received from the output of Box A in figure 2) coupled to the first level shifter and an output coupled to the non-selected section of the CPU and I/O sections, to generate an output data signal (output Q of figure 2) in response to the level shifted data signal and clock signal (Ovens discloses the data signal entering the I/O 202 is level shifted by level shifter 206 and latched by master and slave latches [Box B and transistors M11-M14 in figure 2] to output Q as is also depicted in figures 4a-c; column 5, lines 11-33 and column 5, line 66 thru column 6, line 14).

Ovens does not disclose a second level shifter, coupled to the clock source, to generate a level shifted clock signal in response to the clock signal.

Cairns teaches a level shifting circuit wherein a level shifter (42) is used to shift a clock signal (DCK) from a first voltage level (V_{HH}) to a second voltage level (V_{DD}) (column 8, line 65 thru column 9, line 8). The level shifted clock signal is used to enable a latch circuit (44) that receives data (column 9, lines 36-37). Cairns also has the added benefit of operating in very high speeds and still saving power consumption (column 3, lines 52-57).

It would have been obvious to one of ordinary skill of the art having the teachings of Ovens and Cairns at the time the invention was made, to modify the clocking enable scheme of the latch in the I/O circuit of Ovens to include the clock signal enabling the latch to be level shifted as taught by Cairns such that the same clock signal is used for both the core side and the I/O sides and said clock signal is level shifted before being used on the I/O downstream latch. One of ordinary skill in the art would be motivated to make this combination of level shifting the upstream clock to be used downstream on a latch in view of the teachings of Cairns, as doing so

would give the added benefit of operating in very high speeds and still saving power consumption (column 3, lines 52-57).

As to claim 11, Ovens discloses the apparatus wherein the level shifted clock signal has a plurality of clock cycles with each of the clock cycles having a rising clock edge and a falling clock edge (As is known in the art, clock signals are comprised of perpetual rising and falling edges comprising a plurality of clock cycles); the downstream latch has an open and a close state (As is known in the art, latches are either open to let data flow through or closed to block the transmission of the data); and the downstream latch is switched from the close state to open state by a triggering clock edge selected from the rising clock edge and the falling clock edge (As is shown in Box B of figure 2 by using CLKT and CLKF to latch the transmission gates; column 5, lines 11-24).

As to claim 12, Ovens discloses the apparatus further comprising: a delay element coupled between the clock source and the second level shifter and responsive to the clock signal to provide a delayed clock signal to the second level shifter (Ovens discloses the clock source from the CTS clock synchronizing all clocks by incorporating buffers to balance all clocks as is known in the art; column 3, lines 43-50).

As to claim 13, Ovens discloses the apparatus wherein the level shifted data signal has a plurality of rising and falling data edges (as is known the art with data signals) and the delay element is operable to delay the triggering clock edge until after an arrival of the rising and falling data edges at the second level shifter (column 5, lines 21-33).

As to claim 14, Ovens discloses the apparatus wherein the converter circuit includes a flip-flop having a master latch coupled to the clock source and an upstream slave latch, having

inputs coupled to the master latch and the clock source and an output coupled to the first level shifted, to generate the first data signal; and the downstream latch being a downstream slave latch (column 3, line 62 thru column 4, line 8 and column 5, lines 11-33).

As to claim 15, Ovens discloses the apparatus wherein the selected section generates an input signal; the master latch has an input to receive the input signal; and the flip-flop is operable to generate the first data signal in response to the input signal (column 3, line 62 thru column 4, line 8 and column 5, lines 11-33).

As to claim 16, Ovens discloses a system, comprising: a microprocessor including a central processing unit (CPU) section coupled to a first supply voltage source (V_{DD}) (see figures 1 and 2); an input-output (I/O) section coupled to a second supply voltage source (V_{DDS}) (see figures 1 and 2); a clock source to generate a clock signal (108 of figure 1 or 208 of figure 2; column 3, lines 43-50); and the CPU section being operable to generate a first data signal (Ovens discloses the core 104 providing an input data signal A 204 before processing onto I/O section for outputting; column 4, lines 35-43); a converter circuit including a first level shifter (206), coupled to the selected section (coupled to both the core and the I/O sections); a converter circuit including a first level shifter (206), coupled to the CPU section (coupled to both the core and the I/O sections), to generate a level shifted data signal (signal Y 222 in figure 2) in response to the first data signal (column 4, lines 35-43); and a downstream latch (Box B of figure 2 within the I/O section), having a pair of inputs (clock signals CLKT or CLKF and data signal Y 222 received from the output of Box A in figure 2) coupled to the first level shifter (206) and an output coupled to the I/O section (output Q of figure 2), to generate an output data signal in response to the level shifted data signal and level shifted clock signal (Ovens discloses the data

signal entering the I/O 202 is level shifted by level shifter 206 and latched by master and slave latches [Box B and transistors M11-M14 in figure 2] to output Q as is also depicted in figures 4a-c; column 5, lines 11-33 and column 5, line 66 thru column 6, line 14); a source synchronous bus, coupled to the I/O section, to receive the level shifted data signal and the level shifted clock signal (Ovens discloses the level shifting circuit being part of an integrated circuit [microprocessor] wherein, as is known in the art, is coupled at the I/O pins to a bus to transfer said data/clock signals for synchronization of processing; column 1, lines 11-23); and an I/O module coupled to the source synchronous bus (Though explicitly state an I/O module, Ovens does disclose the output Y 128 of the circuit in figure 1 needing an output buffer to the output pin of the IC which necessitates the need for an I/O module wherein said output is synchronous; column 3, line 66 thru column 4, line 8 and column 2, lines 27-35).

Ovens does not disclose a second level shifter, coupled to the clock source, to generate a level shifted clock signal in response to the clock signal.

Cairns teaches a level shifting circuit wherein a level shifter (42) is used to shift a clock signal (DCK) from a first voltage level (V_{HH}) to a second voltage level (V_{DD}) (column 8, line 65 thru column 9, line 8). The level shifted clock signal is used to enable a latch circuit (44) that receives data (column 9, lines 36-37). Cairns also has the added benefit of operating in very high speeds and still saving power consumption (column 3, lines 52-57).

It would have been obvious to one of ordinary skill of the art having the teachings of Ovens and Cairns at the time the invention was made, to modify the clocking enable scheme of the latch in the I/O circuit of Ovens to include the clock signal enabling the latch to be level shifted as taught by Cairns such that the same clock signal is used for both the core side and the

I/O sides and said clock signal is level shifted before being used on the I/O downstream latch. One of ordinary skill in the art would be motivated to make this combination of level shifting the upstream clock to be used downstream on a latch in view of the teachings of Cairns, as doing so would give the added benefit of operating in very high speeds and still saving power consumption (column 3, lines 52-57).

As to claim 17, Ovens discloses the system wherein the I/O module is a selected one of a graphics and a video controller (Ovens discloses the ICs to include programmable controllers; column 1, lines 11-24).

As to claim 18, Ovens discloses the system wherein the level shifted clock signal has a plurality of clock cycles with each of the clock cycles having a rising clock edge and a falling clock edge (As is known in the art, clock signals are comprised of perpetual rising and falling edges comprising a plurality of clock cycles); the downstream latch has an open and a close state (As is known in the art, latches are either open to let data flow through or closed to block the transmission of the data); and the downstream latch is switched from the close state to open state by a triggering clock edge selected from the rising clock edge and the falling clock edge (As is shown in Box B of figure 2 by using CLKT and CLKF to latch the transmission gates; column 5, lines 11-24).

As to claim 19, Ovens discloses the system further comprising: a delay element coupled between the clock source and the second level shifter and responsive to the clock signal to provide a delayed clock signal to the second level shifter (Ovens discloses the clock source from the CTS clock synchronizing all clocks by incorporating buffers to balance all clocks as is known in the art; column 3, lines 43-50).

As to claim 20, Ovens discloses the system wherein the level shifted data signal has a plurality of rising and falling data edges (as is known the art with data signals) and the delay element is operable to delay the triggering clock edge until after an arrival of the rising and falling data edges at the second level shifter (column 5, lines 21-33).

As to claim 21, Ovens discloses the system wherein the converter circuit includes a flip-flop having a master latch coupled to the clock source and an upstream slave latch, having inputs coupled to the master latch and the clock source and an output coupled to the first level shifted, to generate the first data signal; and the downstream latch being a downstream slave latch (column 3, line 62 thru column 4, line 8 and column 5, lines 11-33).

As to claim 22, Ovens discloses the system wherein the CPU section generates an input signal; the master latch has an input to receive the input signal; and the flip-flop is operable to generate the first data signal in response to the input signal (column 3, line 62 thru column 4, line 8 and column 5, lines 11-33).

Claims 2-9 and 25-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ovens et al. (U.S. Patent No. 6,351,173 B1) (hereinafter referred to as Ovens) as applied to claims 1 and 23-24 above, and further in view of Cairns et al. (U.S. Patent No. 6,806,734 B2) (hereinafter referred to as Cairns).

As to claim 2, Ovens fails to disclose the apparatus further comprising: a second level shifter, coupled between the clock source and the downstream latch, to generate a level shifted clock signal in response to the clock signal; and the downstream latch, having the pair of inputs coupled to the first level shifter and the second level shifter, to generate the output data signal in response to the level shifted data signal and the level shifted clock signal.

Cairns teaches a level shifting circuit wherein a level shifter (42) is used to shift a clock signal (DCK) from a first voltage level (V_{HH}) to a second voltage level (V_{DD}) (column 8, line 65 thru column 9, line 8). The level shifted clock signal is used to enable a latch circuit (44) that receives data (column 9, lines 36-37). Cairns also has the added benefit of operating in very high speeds and still saving power consumption (column 3, lines 52-57).

It would have been obvious to one of ordinary skill of the art having the teachings of Ovens and Cairns at the time the invention was made, to modify the clocking enable scheme of the latch in the I/O circuit of Ovens to include the clock signal enabling the latch to be level shifted as taught by Cairns such that the same clock signal is used for both the core side and the I/O sides and said clock signal is level shifted before being used on the I/O downstream latch wherein the downstream latch inputs include the level shifted data from the first level shifter and the level shifted clock signal from the second level shifter. One of ordinary skill in the art would be motivated to make this combination of level shifting the upstream clock to be used downstream on a latch in view of the teachings of Cairns, as doing so would give the added benefit of operating in very high speeds and still saving power consumption (column 3, lines 52-57).

As to claim 3, Ovens discloses the apparatus wherein the level shifted clock signal has a plurality of clock cycles with each of the clock cycles having a rising clock edge and a falling clock edge (As is known in the art, clock signals are comprised of perpetual rising and falling edges comprising a plurality of clock cycles); the downstream latch has an open and a close state (As is known in the art, latches are either open to let data flow through or closed to block the transmission of the data); and the downstream latch is switched from the close state to open state

by a triggering clock edge selected from the rising clock edge and the falling clock edge (As is shown in Box B of figure 2 by using CLKT and CLKF to latch the transmission gates; column 5, lines 11-24).

As to claim 4, Ovens discloses the apparatus wherein the level shifted clock signal has a plurality of clock cycles with each of the clock cycles having a rising clock edge and a falling clock edge (As is known in the art, clock signals are comprised of perpetual rising and falling edges comprising a plurality of clock cycles); the downstream latch has an open and a close state (As is known in the art, latches are either open to let data flow through or closed to block the transmission of the data); and the downstream latch is switched from the close state to open state by a triggering clock edge selected from the rising clock edge and the falling clock edge and switched from the open state to a close state by the non-selected clock edge of the rising clock edge and the falling clock edge (As is known in the art by way of a positive or negative flip-flop storage latch. As is shown in Box B of figure 2 by using CLKT and CLKF to latch the transmission gates; column 5, lines 11-24).

As to claim 5, Ovens discloses the apparatus further comprising: a delay element coupled between the clock source and the second level shifter and responsive to the clock signal to provide a delayed clock signal to the second level shifter (Ovens discloses the clock source from the CTS clock synchronizing all clocks by incorporating buffers to balance all clocks as is known in the art; column 3, lines 43-50).

As to claim 6, Ovens discloses the apparatus wherein the level shifted data signal has a plurality of rising and falling data edges (as is known the art with data signals) and the delay

element is operable to delay the triggering clock edge until after an arrival of the rising and falling data edges at the second level shifter (column 5, lines 21-33).

As to claim 7, Ovens discloses the apparatus wherein the level shifted data signal has a plurality of rising and falling data edges (as is known the art with data signals) and the delay element is operable to introduce a predetermined delay having a duration exceeding a time period during which the rising and falling data edges are mismatched (column 5, lines 21-33).

As to claim 8, Ovens discloses the apparatus further comprising: a flip-flop, coupled to the first circuit, including a master latch coupled to the clock source and an upstream slave latch, having inputs coupled to the master latch and the clock source and an output coupled to the first level shifted, to generate the first data signal; and wherein the downstream latch is a downstream slave latch (column 3, line 62 thru column 4, line 8 and column 5, lines 11-33).

As to claim 9, Ovens discloses the apparatus wherein the first circuit generates an input signal; the master latch has an input to receive the input signal; and the flip-flop is operable to generate the first data signal in response to the input signal (column 3, line 62 thru column 4, line 8 and column 5, lines 11-33).

As to claim 25, Ovens fails to disclose the method further comprising: shifting the clock signal from the first supply voltage to the second supply voltage by way of a second level shifter to generate a level shifted clock signal having the rising clock edge and the falling clock edge.

Cairns teaches a level shifting circuit wherein a level shifter (42) is used to shift a clock signal (DCK) from a first voltage level (V_{HH}) to a second voltage level (V_{DD}) (column 8, line 65 thru column 9, line 8). The level shifted clock signal is used to enable a latch circuit (44) that

receives data (column 9, lines 36-37). Cairns also has the added benefit of operating in very high speeds and still saving power consumption (column 3, lines 52-57).

It would have been obvious to one of ordinary skill of the art having the teachings of Ovens and Cairns at the time the invention was made, to modify the clocking enable scheme of the latch in the I/O circuit of Ovens to include the clock signal enabling the latch to be level shifted as taught by Cairns such that the same clock signal is used for both the core side and the I/O sides and said clock signal is level shifted before being used on the I/O downstream latch wherein the downstream latch inputs include the level shifted data from the first level shifter and the level shifted clock signal from the second level shifter. One of ordinary skill in the art would be motivated to make this combination of level shifting the upstream clock to be used downstream on a latch in view of the teachings of Cairns, as doing so would give the added benefit of operating in very high speeds and still saving power consumption (column 3, lines 52-57).

As to claim 26, Ovens discloses the method further comprising: delaying the clock signal by a predetermined amount exceeding a period of time during which the plurality of rising and falling data edges are mismatched (Ovens discloses the clock source from the CTS clock synchronizing all clocks by incorporating buffers to balance all clocks as is known in the art; column 3, lines 43-50).

As to claim 27, Ovens discloses the method further comprising: delaying an input signal by a single clock cycle of the clock signal with a flip-flop having a master latch and a slave latch to generate a delayed input signal; and providing the delayed input signal to the first level shifter (Ovens discloses a master and slave latch available; column 4, lines 50-59).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to James Sugent whose telephone number is (571) 272-5726. The examiner can normally be reached on 8AM - 4PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Browne can be reached on (571) 272-3670. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at (866) 217-9197 (toll-free).

LYNNE H. BROWNE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100

James Sugent
Patent Examiner, Art Unit 2116
May 16, 2006